19-1855 Rev 0; 11/00

MAXIM

+3.3V, 2.5Gbps Quad Transimpedance Amplifier for System Interconnects

General Description

The MAX3825 is a quad transimpedance amplifier (TIA) intended for 2.5Gbps system interconnect applications. Each of the four channels converts a small photodiode current to a measurable differential voltage with a transimpedance gain of 3.7kΩ. The circuit features 460nA$_{RMS}$ of input-referred noise per channel corresponding to an optical input sensitivity of -22.3dBm (BER ≤ 1×10^{-14}). The quad transimpedance amplifier has 20ps of deterministic jitter and a 2.4GHz small-signal bandwidth. The MAX3825 is optimized for use with a quad PIN photodetector array with a standard fiber pitch of 250µm.

The MAX3825 operates from a single +3.3V supply over a 0°C to +85°C temperature range. With a +3.3V supply, each channel dissipates 93mW of power. A DC cancellation circuit on each channel provides a true differential output swing over a wide range of input currents.

Each channel has an independent supply and ground to allow all or any combination of channels to be connected. This device is available in dice only.

Typical Operating Circuit appears at end of data sheet.

Features

- **Single +3.3V Supply**
- **93mW per Channel Power Dissipation**
- **460nA$_{RMS}$ Input-Referred Noise**
- **20ps Deterministic Jitter**
- **2.4GHz Small-Signal Bandwidth**
- **No External Compensation**
- **40dB Power-Supply Rejection Ratio**
- **Compact Die with 250µm Channel Pitch**
- **100Ω Differential Output Impedance**

Ordering Information

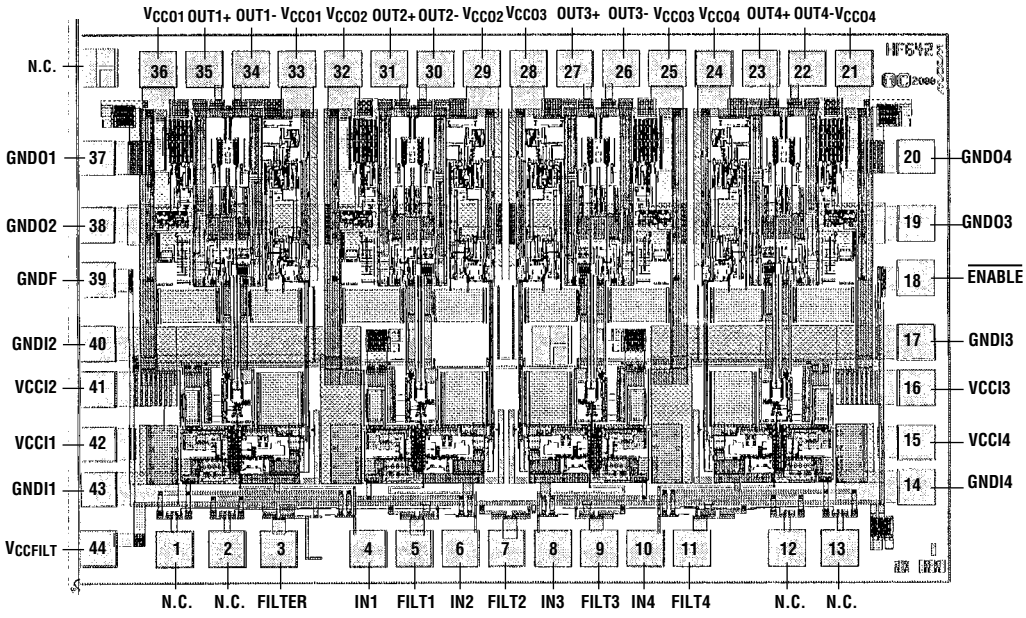
PART	TEMP. RANGE	PIN-PACKAGE
MAX3825U/D	0°C to +85°C	Dice*

**Dice are designed to operate with a 0°C to +120°C junction temperature, but are tested and guaranteed only at T_A = +25°C.*

Applications

System Interconnects
SDH/SONET Backplanes
Dense Digital Cross-Connects
ATM Switching Networks
High-Speed Parallel Optical Links

Chip Topography/Pad Configuration



+3.3V, 2.5Gbps Quad Transimpedance Amplifier for System Interconnects

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V_{CCO1}, V_{CCO2}, V_{CCO3}, V_{CCO4},
V_{CCI1}, V_{CCI2}, V_{CCI3}, V_{CCI4}, V_{CCFILT} .....-0.5V to +6.0V
Input Current: IN1, IN2, IN3, IN4.....-4mA to +4mA
FILTER Current.....-24mA to +24mA
Filter Current: FILT1, FILT2, FILT3, FILT4 .....-6mA to +6mA

Output Voltage OUT1±, OUT2±,
OUT3±, OUT4±.....(V_{CC} - 1.5V) to (V_{CC} + 0.5V)
$\overline{ENABLE}$ Voltage.....-0.5V to (V_{CC} + 0.5V)
Operating Temperature Range (T_A).....0°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Operating Junction Temperature (T_J).....-55°C to +150°C
Processing Temperature.....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.14V to +3.6V, T_A = 0°C to +85°C. Typical values are at +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	Single channel		28	40	mA
		Dual channel		56	80	
		Quad channel		112	160	
Input Bias Voltage		I_{IN} = 0		0.89	0.99	V
DC Input Overload			1.7			mA
Transimpedance	Z_{21}	10µAp-p, 100 Ω differential load	3.0	3.7	4.5	kΩ
Filter Resistor RFILTER	R_{FILTER}			180		Ω
Filter Resistors RFILT1–4	$R_{FILT\_}$			720		Ω
Single-Ended Output Impedance	R_O		43	50	57	Ω
Transimpedance Linear Range		(Note 1)	50			µAp-p
Maximum Differential Output Range		I_{IN} = 2mAp-p	230	340	480	mVp-p
Output Offset Voltage	V_{offset}	I_{IN} = 10µAp-p	-5		+5	mV
Output Common Mode Voltage		50Ω loads to V_{CC}		V_{CC} - 0.09		V

Note 1: Gain at 50µAp-p is within 10% of the small signal gain.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.14V to +3.6V, T_A = 0°C to +85°C. Typical values are at +3.3V, T_A = +25°C, unless otherwise noted. Total source capacitance = 0.7pF.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC Input Overload		(Note 3)	2			mAp-p
Input Referred Noise	I_N			460	600	nA_{rms}
Low-Frequency Cutoff		(Note 4)		60	100	kHz
Deterministic Jitter (Note 5)	DJ	I_{IN} > 100µAp-p		20	45	ps
Power-Supply Rejection Ratio	PSRR	(Note 6)		40		dB
Small-Signal Bandwidth	BW			2.4		GHz
Maximum Skew (Note 7)		Any two channels within a chip			50	ps

AC ELECTRICAL CHARACTERISTICS (continued)

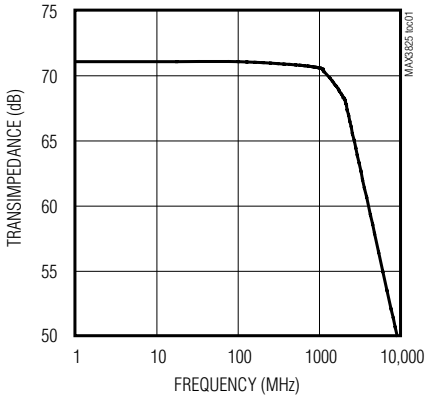
(V_{CC} = +3.14V to +3.6V, T_A = 0°C to +85°C. Typical values are at +3.3V, T_A = +25°C, unless otherwise noted. Total source capacitance = 0.7pF.) (Note 2)

Note 2: AC characteristics are guaranteed by design and characterization.
Note 3: The maximum input current is specified with output deterministic jitter ≤ 45ps.
Note 4: No external compensation capacitors are used. Measured with I_{IN} = 30μA_{avg}.
Note 5: Deterministic jitter is the arithmetic sum of pattern-dependent jitter and pulse width distortion. Measured with a 2^{13} -1 PRBS with 100 consecutive 0s and 100 consecutive 1s applied to a single channel. See *Typical Operating Characteristics*.
Note 6: PSRR = -20log(ΔV_{OUT} / $V_{noise(on\ VCC)}$), f ≤ 2MHz. Measured by applying DC current = 30µA, and applying 100mVp-p signal at power supply.
Note 7: Measured by applying the same input signal to all channels. Skew measurements are made at the 50% point of the transition.

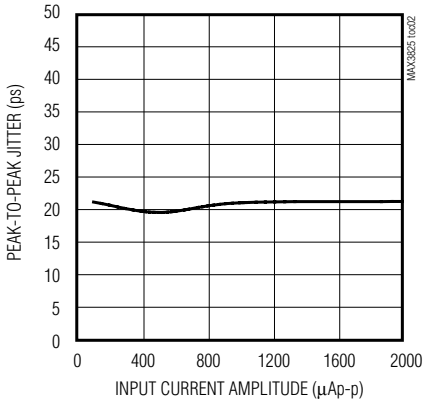
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

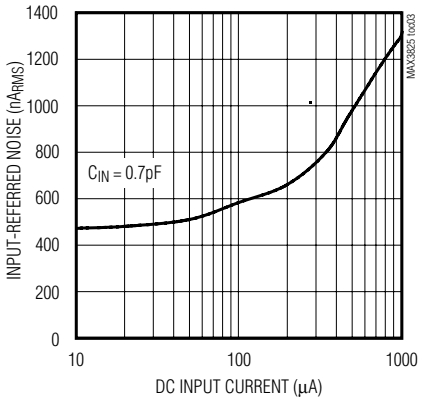
FREQUENCY RESPONSE



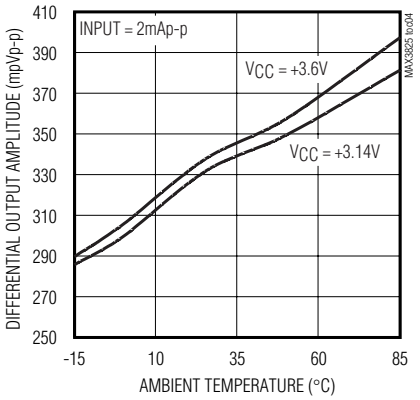
DETERMINISTIC JITTER vs. INPUT AMPLITUDE



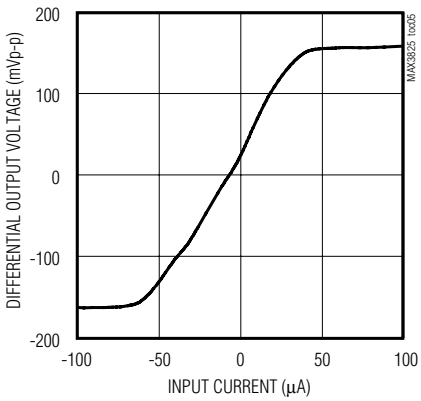
INPUT-REFERRED RMS NOISE CURRENT vs. DC INPUT CURRENT



DIFFERENTIAL OUTPUT AMPLITUDE vs. TEMPERATURE



DC TRANSFER FUNCTION

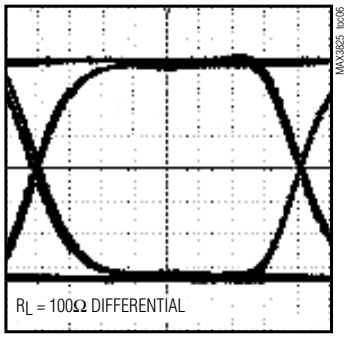


+3.3V, 2.5Gbps Quad Transimpedance Amplifier for System Interconnects

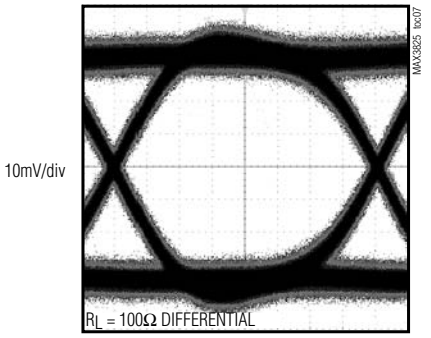
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

ELECTRICAL EYE DIAGRAM
INPUT = 2mAp-p, 2.5Gbps, 2^{13} - 1 PRBS



ELECTRICAL EYE DIAGRAM
INPUT = 20μAp-p, 2.5Gbps, 2^{13} - 1 PRBS



Pad Description

PAD	NAME	FUNCTION
1, 2, 12, 13	N.C.	No Connection. Leave open and unconnected.
3	FILTER	Connection to internal 180Ω Filter Resistor to V_{CCFILT} for Photodiode Array Cathode Bias
4, 6, 8, 10	IN1 to IN4	Signal Inputs. Channel 1 to channel 4 signal inputs.
5, 7, 9, 11	FILT1 to FILT4	Filter Connections. Channel 1 to channel 4 connection to internal filter resistors (720Ω to V_{CCFILT}).
14, 17, 40, 43	GNDI4 to GNDI1	Input Stage Ground Connections. Channel 4 to channel 1 input stage ground.
15, 16, 41, 42	V_{CCI4} to V_{CCI1}	Input Stage Supply Connections. Channel 4 to channel 1 input stage positive supply.
18	$\overline{\text{ENABLE}}$	DC Feedback Disable. Disables DC feedback of all four channels when connected to the positive supply (V_{CC}). Left unconnected for normal operation.
20, 19, 38, 37	GNDO4 to GNDO1	Output Stage Ground Connections. Channel 4 to channel 1 output stage ground.
21, 24	V_{CCO4}	Channel 4 Output Stage Positive Supply
22, 26, 30, 34	OUT4- to OUT1-	Inverting Outputs. Channel 4 to channel 1 negative outputs.
23, 27, 31, 35	OUT4+ to OUT1+	Noninverting Outputs. Channel 4 to channel 1 positive outputs.
25, 28	V_{CCO3}	Channel 3 Output Stage Positive Supply
29, 32	V_{CCO2}	Channel 2 Output Stage Positive Supply
33, 36	V_{CCO1}	Channel 1 Output Stage Positive Supply
39	GNDF	Ground Connection for the Filters. Filter grounds.
44	V_{CCFILT}	Power Supply Connection for Filter Resistor

Functional Diagram

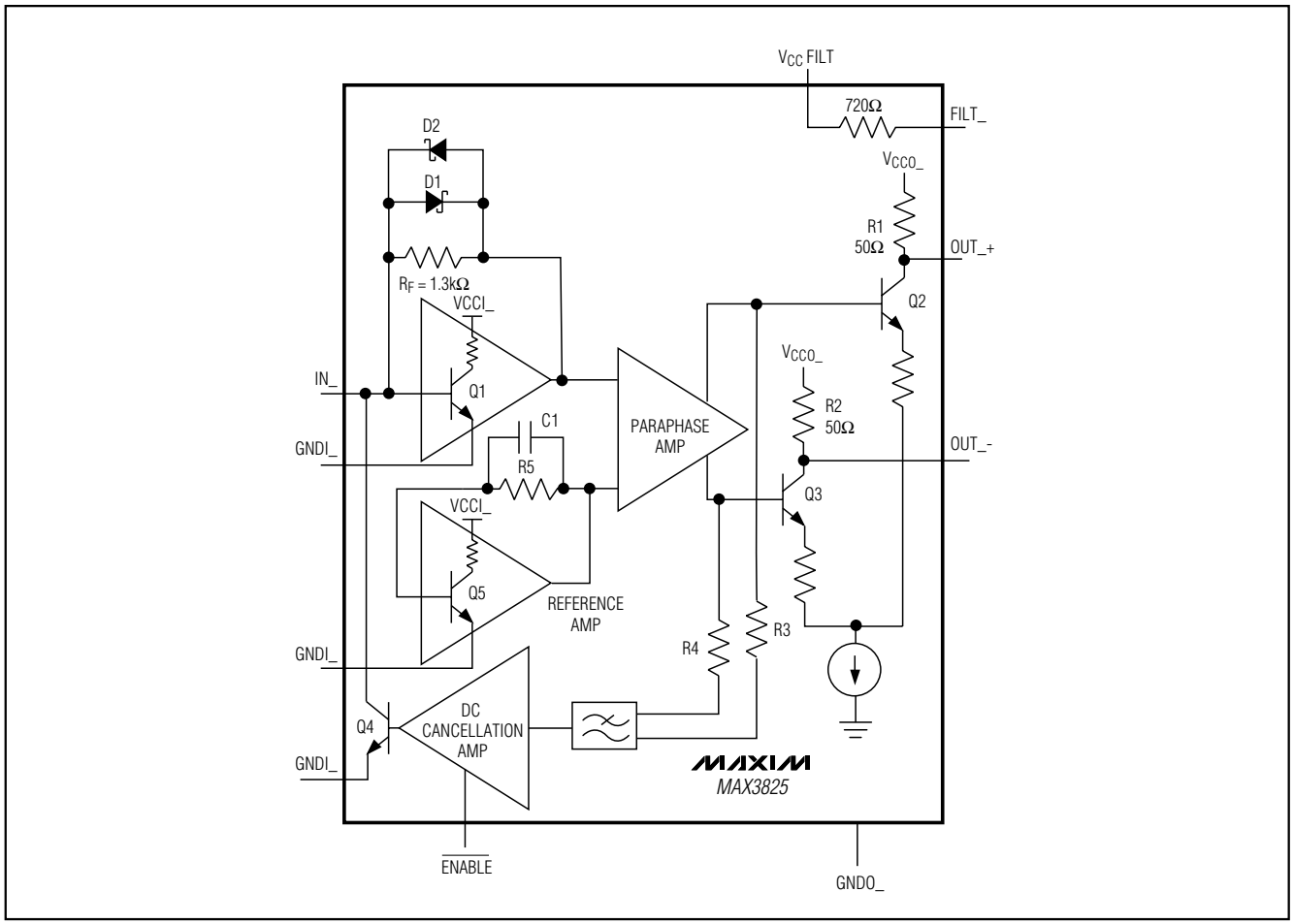


Figure 1. Functional Diagram for One Channel of the MAX3825

Detailed Description

The MAX3825 quad TIA circuit is designed for 2.5Gbps SONET/SDH applications. It comprises a transimpedance amplifier, a paraphase amplifier with CML outputs, and a DC cancellation loop to reduce pulse-width distortion (Figure 1).

Transimpedance Amplifier

The signal current at IN_ flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage with a gain of 1300Ω. Diodes D1 and D2 clamp the output voltage for large input currents. GNDI_ is a direct connection to the emitter of the input transistor and must be connected directly to the photodetector AC ground return for best performance.

DC Cancellation Loop

The DC cancellation loop removes the DC component of the input signal by using low-frequency feedback. This feature centers the signal within the MAX3825's dynamic range, reducing pulse-width distortion.

The output of the paraphrase amplifier is sensed through resistors R3 and R4 and then filtered, amplified, and fed back to the base of transistor Q4. The transistor draws the DC component of the input signal away from the transimpedance amplifier's summing node.

The MAX3825 DC cancellation loop is internally compensated and does not require external capacitors in most 2.5Gbps applications. The DC cancellation loop for all channels can be disabled by connecting $\overline{ENABLE}$ to the positive supply (V_{CC}). $\overline{ENABLE}$ is inter-

+3.3V, 2.5Gbps Quad Transimpedance Amplifier for System Interconnects

nally pulled low, so it does not need to be bonded out for the DC cancellation loop to function.

The MAX3825 minimizes pulse-width distortion for data sequences exhibiting a 50% duty cycle and mark density. An input signal with a duty cycle and mark density significantly different from 50% will cause the MAX3825 to operate improperly.

DC cancellation current drawn from the input creates noise. This is not a problem for a low-level signal with little or no DC component. Preamplifier noise increases for a signal with significant DC component (see *Typical Operating Characteristics*).

Paraphase Amplifier and Output Stage

The paraphase amplifier converts single-ended inputs to differential outputs, and introduces a voltage gain of 2.8. This signal drives an internally biased emitter coupled pair, Q2 and Q3, which forms the output stage (Figure 1). Resistors R1 and R2 provide back-termination at the outputs, absorbing reflections between the MAX3825 and its load.

The differential outputs are designed to drive a 100Ω load between OUT_+ and OUT_-. The MAX3825 can also drive higher output impedances, resulting in increased gain and output voltage swing.

Applications Information

The MAX3825 is a quad TIA that is ideal for 2.5Gbps SONET/SDH receivers. Its features allow easy design into a fiberoptic module.

Optical Power Relations

Many of the MAX3825 specifications relate to the input signal amplitude. When working with fiberoptic receivers, the input is usually expressed in terms of average optical power and extinction ratio. Table 1 shows relations that are helpful for converting optical power to an input signal when designing with the MAX3825 (Figure 2). The definitions are true if the mark density and duty cycle of the input data are 50%.

Optical Sensitivity Calculation

The input-referred RMS noise current (I_N) of the MAX3825 generally determines the receiver sensitivity. To obtain a system bit error rate (BER) of 1×10^{-14}, the signal-to-noise ratio must always exceed 15.3. The input sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\log_{10}\left(\frac{15.3 I_N (r_e + 1)}{2\rho(r_e - 1) \times 1000}\right)$$

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P_0 + P_1)/2$
Extinction Ratio	r_e	$r_e = P_1/P_0$
Optical Power of a "1"	P_1	$P_1 = 2P_{AVG}(r_e)/(r_e + 1)$
Optical Power of a "0"	P_0	$P_0 = 2P_{AVG}/(r_e + 1)$
Signal Amplitude	P_{IN}	$P_{IN} = P_1 - P_0 = 2P_{AVG}$ $(r_e - 1)/(r_e + 1)$

***Note**: Assuming a 50% input duty cycle and mark density*

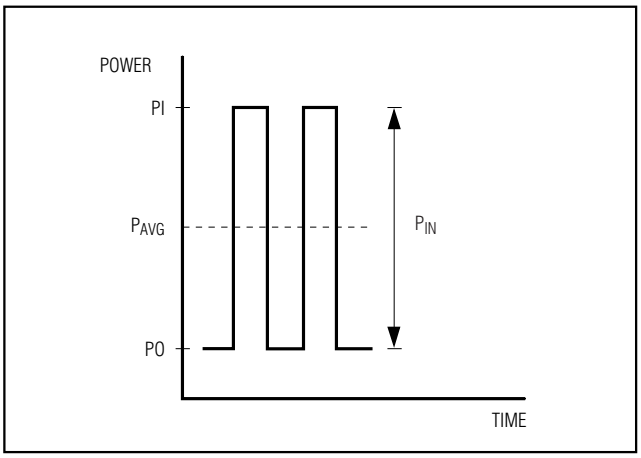


Figure 2. Optical Power Definitions

where ρ is the photodiode responsivity in A/W and I_N is in µA.

Input Optical Overload

The overload is the largest input that the MAX3825 accepts while meeting specifications. The optical overload can be estimated in terms of average power with the following equation:

$$\text{Overload} = 10\log_{10}\left(\frac{I_{MAX}}{2\rho}\right)\text{dBm}$$

where ρ is the photodiode responsivity in A/W and I_{MAX} is in mA.

Optical Linear Range

The MAX3825's outputs limit when the input signal exceeds 50µAp-p. The MAX3825 operates in a linear range for inputs not exceeding:

$$\text{Linear Range} = 10\log_{10}\left(\frac{50\mu A(r_e+1)}{2\rho(r_e-1)\times 1000}\right)\text{dBm}$$

where ρ is the photodiode responsivity in A/W.

Ground

Connect all input ground connections as close as possible to the AC ground of the photodetector diode. The photodetector AC ground is usually the ground of the filter capacitor from the photodetector cathode. The total loop (from GNDI_, through the bypass capacitor and the diode, and back to IN_) should be as short as possible.

Photodiode Filter

Supply voltage noise at the cathode of the photodiode produces a current I = C_{PD} ΔV/Δt, which reduces the receiver sensitivity (C_{PD} is the photodiode capacitance). The filter resistor of the MAX3825, combined with an external capacitor, can be used to reduce this noise (see the *Typical Application Circuit*). Current generated by the supply noise voltage is divided between C_{FILTER} and C_{PD}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = \frac{(V_{NOISE})(C_{PD})}{(R_{FILTER})(C_{FILTER})}$$

Another important parameter is the inductance at the photodiode array's common cathode. It is important to keep this inductance to a minimum to reduce the coupling between the photodiodes. To keep this inductance small, keep all bond wires as short as possible.

Wire Bonding

For high current density and reliable operation, the MAX3825 uses gold metalization. Connections to the die should be made with gold wire only, using ball bonding techniques. Wedge bonding is not recommended. Die thickness is typically 14 mils (mm).

Interface Models

Refer to Figures 3 and 4 for the equivalent input and output circuits of the MAX3825.

Chip Information

TRANSISTOR COUNT: 1469

PROCESS: BIPOLAR (SILICON GERMANIUM)

DIE SIZE: 65 × 99mils/(1651 × 2515 microns)

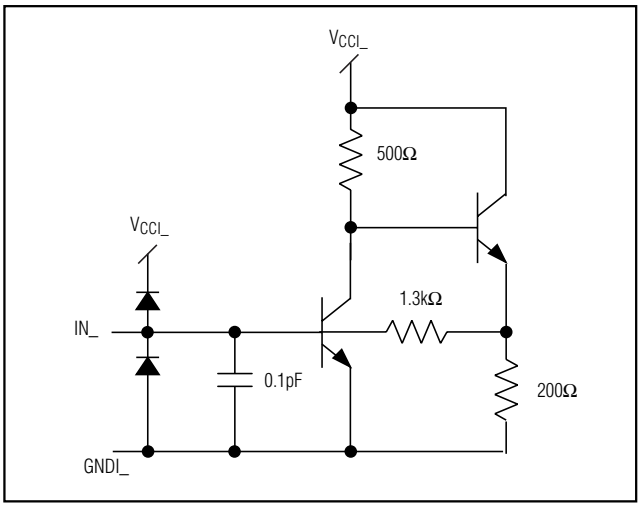


Figure 3. Equivalent Input Circuit

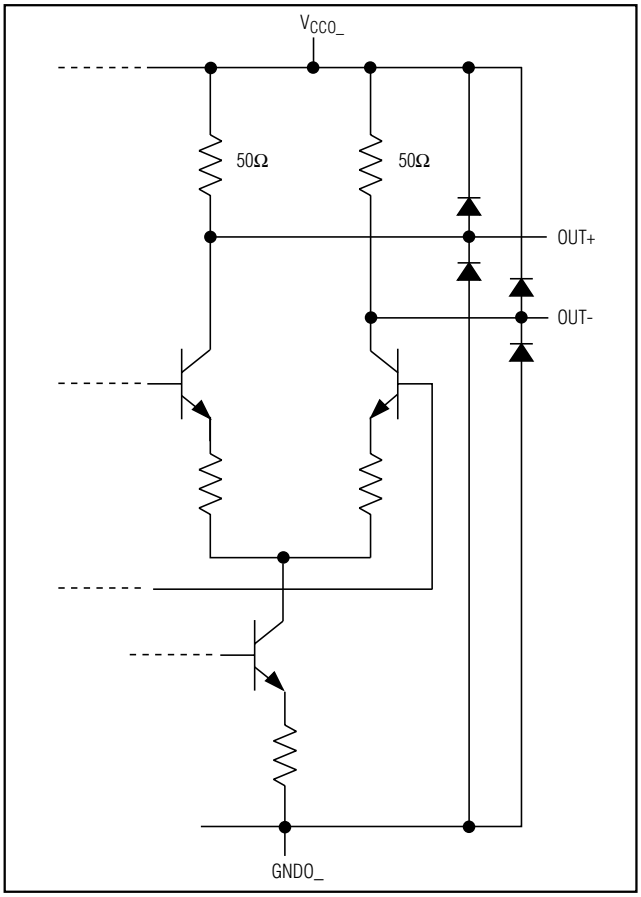


Figure 4. Equivalent Output Circuit

+3.3V, 2.5Gbps Quad Transimpedance Amplifier for System Interconnects

Typical Application Circuit